

Zhihan Xu

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<https://zhihanxu.github.io>

EDUCATION

Ph.D. in Computer Engineering University of Southern California Overall GPA: 3.85/4.0	08/2023-Now CA, United States
M.Sc. in Electrical Engineering University of Pennsylvania Overall GPA: 3.84/4.0, Track: Circuits and Computer Engineering	09/2021-05/2023 PA, United States
B.Eng. with Honors of the First Class in Electronics and Electrical Engineering University of Glasgow (UoG)	09/2016-06/2020 Glasgow, United Kingdom
B.Eng. in Electronic Information Engineering University of Electronic Science and Technology of China (UESTC) Overall GPA: 3.7/4.0, Outstanding Graduate in UESTC (Distinction)	09/2016-06/2020 Chengdu, China

RESEARCH INTERESTS

FPGA Accelerator, High-level Synthesis (HLS), Heterogeneous/Parallel Computing, Fully Homomorphic Encryption

PUBLICATIONS

- Bandwidth Efficient Homomorphic Encrypted Discrete Fourier Transform Acceleration on FPGA (1st Author)
2024 IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)
- N³H-Core: Neuron-designed Neural Network Accelerator via FPGA-based Heterogeneous Computing Cores (1st Author)
2022 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
- IoT Enabled Smart Security Framework for 3D Printed Smart Home (1st Author)
2020 IEEE International Conference on Smart Internet of Things (SmartIoT)
- High- and Low-Level Feature Enhancement for Medical Image Segmentation
2019 International Workshop on Machine Learning in Medical Imaging (MLMI)

EMPLOYMENT

Teaching Assistant, USC <ul style="list-style-type: none">EE354 Introduction to Digital Circuits	01-05/2024
Research Assistant, USC <ul style="list-style-type: none">Fully Homomorphic Encryption Acceleration on FPGA at FPGA/Parallel Computing Lab	08/2023-Now
Teaching Assistant, UPenn <ul style="list-style-type: none">ESE5310 Digital Signal Processing	01-05/2023
GPU Design Verification Intern, NVIDIA Corporation (US) <ul style="list-style-type: none">Summer Intern at Streaming Multiprocessor (SM) Design Verification Team focusing on testlist optimizationDesigned and deployed Baysian Optimization flow on testlists to improve test coverage. The algorithm explores the knob space and tunes knob values with a test result feedback loop to improve the hitrate on specific targetsImplemented a NN trained with random tests, which accelerates the BayOpt flow to generate optimized testlists	05-08/2022
Research Assistant, advised by Prof. Li Jiang, Shanghai Jiao Tong Univ. & Shanghai Qi Zhi Institute <ul style="list-style-type: none">Neural network (NN) compression and design space exploration on the FPGA-based NN accelerator.Full-time worked in the Advanced Computer Architecture (ACA) lab at Shanghai Jiao Tong University (SJTU).	09/2020-07/2021

EXPERIENCES

- Design of Configurational Logic Block (CLB) in FPGA, UPenn** 11-12/2022
- Design the circuit-level implementation of a CLB with a 16:1 Look-up Table (LUT) using pass transistor logic for multiplexers optimized for the delay, with control logic to load the 6-T SRAM cells holding a custom truth table.
- Processor Design with Superscalar Pipelined Datapath, UPenn** 02-05/2022
- Designed a superscalar with two in-order pipelines for LC4 ISA, with multi-ported and bypassed register file.
 - Designed the stalling logic, squash logic, and bypassing logic for pipeline switch. Tested the processor on Zedboard.
- Accelerating VGG16 DCNN with a cloud FPGA, advised by Prof. Jing (Jane) Li, UPenn** 11-12/2021
- Designed a VGG16 accelerator under heterogeneous computing framework OpenCL with AWS EC2 F1 Instance.
 - Applied General Matrix Multiplication (GEMM) algorithm in C++ OpenCL host code binded with Pytorch and systolic array kernel for matrix multiplications on FPGA. Optimized the kernel with HLS pragmas like array partition.
- Data Compressor Design and Acceleration on the Heterogeneous Platform Ultra96, UPenn** 10-12/2021
- Designed a compressor receiving data in real-time and reducing data size by identifying and reducing redundancy.
 - Implemented the flow with content-defined chunking, SHA-384 deduplication, and LZW compression steps.
 - Achieved C solution on the Single ARM Processor first. Identified performance bottlenecks and mapped the bottleneck functions on the FPGA logic. Optimized the throughput with data streaming, loop unrolling, pipeline, etc.
- N³H-Core (FPGA '22), advised by Prof. Li Jiang, Advanced Computer Architecture (ACA) Lab at SJTU** 09/2020-07/2021
- Designed a heterogeneous DNN accelerator architecture called N³H-Core that consists of DSP- and LUT-centric computing units (aka. DSP-core and LUT-core) to fully exploit the on-chip resource of the target FPGA.
 - Constructed scalable and adaptable cost model across different DNNs and FPGA to precisely estimate the resource utilization, inference latency, and other metrics-of-interests for further design space exploration.
 - Applied the Reinforcement Learning (RL) technique to build the end-to-end optimization framework that automatically generates the architecture configurations (resource), dataflow (both cores), and DNN respectively.
- IoT Smart Home Design for Security (SmartIoT '20), advised by Dr. Qammer H. Abbasi, UoG** 12/2019-04/2020
- Designed an MCU-based smart home with a visual-intelligent surveillance system supported by the Raspberry Pi.
 - Correlated the surveillance system with the door lock system innovatively to further enhance smart security.
- Medical Image Segmentation (MLMI '19), advised by Prof. Guotai Wang, UESTC** 09-12/2019
- Implemented different fully convolutional networks (FCNs) as baseline models and compared their model size and accuracy on two challenging medical image segmentation datasets – skin lesions and spleen.
 - Proposed HLE-Net that utilizes the attention mechanism to selectively aggregate the optimal feature information and uses global semantic information to enhance the semantic consistency of high- and low-level features.

HONORS & AWARDS

- Outstanding Teaching Award in Penn Engineering** 05/2023
- Outstanding Graduate in UESTC (Distinction)** 12/2019
- Outstanding Student Leadership Scholarship** 11/2019
- Outstanding Student Scholarship in UESTC (Top 10%)** 10/2017 10/2018 10/2019
- Honorable Mention of 2019 Mathematical Contest in Modeling (MCM)** 04/2019

SERVICES

- Reviewer:** TVLSI '24
- Sub-reviewer:** H2RC '23, TETC '23, TC '24, HPEC '24
- Conference Organizer:** Proceeding Chair for HiPC '24